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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,597	12/31/2001	Howard S. David	42390.P13871	2206

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,597	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 6 lines 4-5, "the DRAM is placed on a motherboard rather that on a memory module" should be -- the DRAM is placed on a motherboard rather than on a memory module--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 1, Saulsbury discloses an apparatus (104, figure 2) comprising a plurality of tag units, i.e., instruction cache bank tag storage (132) and primary data cache bank tag storage (148), each tag unit including an array of tag address storage locations, the plurality of tag units to perform tag look-up operations (col. 4 lines 45-56 and col. 7 lines 42-61), a memory module decode unit, i.e., row decoder (124, figure 2), the memory module decode unit to perform decode operations in parallel with the tag look-up operations (col. 9 line 54 through

col. 10 line 25), and a command sequencer and serializer unit, i.e., primary data cache bank logic (150) coupled to the array of tag address storage locations, i.e., primary data cache bank tag/flag storage (148), the command sequencer and serializer unit to control a plurality data caches, i.e., primary data cache bank line storage (144), each data cache associated with one of a plurality of memory modules, i.e., memory bank N (118).

Regarding claim 2, Saulsbury discloses each of the plurality of tag units corresponding to one of the plurality of memory modules (col. 7 lines 42-61).

Regarding claim 3, Saulsbury discloses the tag look-up operations to provide cache hit information (col. 9 line 54 through col. 10 line 21).

Regarding claim 4, Saulsbury discloses the tag look-up operations to provide cache line modified information, i.e., tag look-up operations including command to check whether the corresponding cache line contains dirty flag, if it does, a new primary data cache line is replaced (col. 11 line 47 through col. 12 line 64).

Regarding claim 5, Saulsbury discloses each of the arrays of tag address storage locations organized into a plurality of ways (col. 3 lines 54-63).

Regarding claim 6, Saulsbury discloses the tag look-up operations to provide way information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 7, Saulsbury discloses each of the arrays of tag address storage locations organized into 4 ways (col. 3 lines 54-63).

Regarding claim 8, Saulsbury discloses the command sequencer and serializer unit to control the plurality of data caches associated with the plurality of memory modules by

delivering commands over a plurality of command and address lines, i.e., cache lines (4096), buffer control lines, W/R control line and address line (A20-A9) as show in figure 2.

Regarding claim 9, Saulsbury discloses the apparatus wherein the plurality of command and address lines are part of a point-to-point interconnection (figure 2, and col. 3 line 55 through col. 4 line 10).

Regarding claim 16, Saulsbury discloses a method comprising receiving a read request at a memory controller, i.e., data cache bank logic (150, figure 2), performing a tag look-up within the memory controller to determine whether there is a cache hit for the read request, determining which of a plurality of memory modules is addressed by the read request, where in performing a tag look-up and determining which of a plurality of memory modules is addressed by the read request occur in parallel, and fetching a line of cache data from a data cache located on one of the plurality of memory modules if the tag look-up indicates a cache hit (col. 9 line 54 through col. 10 line 21 and col. 11 lines 15-39).

Regarding claim 17, Saulsbury discloses a method wherein performing a tag look-up includes providing way information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 18, Saulsbury discloses a method wherein performing a tag look-up operation includes providing cache line modified information, i.e., tag look-up operations including command to check whether the corresponding cache line contains dirty flag, if it does, a new primary data cache line is replaced (col. 11 line 47 through col. 12 line 64).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westberg (US PAT. 5,361,391) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 10, Westberg discloses a system (10, figure 1) comprising a processor (12, figure 1), a memory controller (14, figure 1) coupled to the processor via the address and data bus (22 and 24, respectively), the memory controller including a plurality of tag units (tag array 30a and 30n, figure 2), each tag unit including an array of tag address storage locations, the plurality unites to perform tag look-up operations (col. 4 lines 34-45 and lines 54-59), a command sequencer and serialize unit, i.e., control logic (28, figure 2) coupled to the array of tag address storage locations (figure 2 and col. 4 line 47 through col. 5 line 7), a plurality of memory modules (32a and 32b, figure 2) coupled to the memory controller via the address bus, data bus and control signal bus. Westberg differs from the claimed invention in not specifically teaches the system comprising a memory module decode unit, the memory module decode unit to perform decode operations in parallel with the tag look-up operations and the plurality of memory modules including a memory device and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller. However, Saulsbury discloses the computer system (100, figure 1) comprising a memory device wherein the memory device including a plurality of memory modules, i.e., memory block (104), each memory module further including a memory module decode unit, i.e., row decoder (124) which

perform decode operations in parallel with the tag look-up operations (col. 9 line 54 through col. 10 line 25), and the memory module further including a memory device, i.e., memory bank N (118) and a data cache (144) wherein the data cache coupled to the memory device via the cache line bus (4096, figure 2), and the data cache controlled by commands, i.e., cache line buses and buffer control buses (figure 2), delivered by the memory controller, i.e., data cache bank logic (150) and (col. 7 lines 21-41 and col. 11 line 15 through col. 12 line 6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Westberg in having a memory module decode unit which perform decode operations in parallel with the tag look-up operations and the plurality of memory modules including a memory device and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 11, Saulsbury discloses a point-to-point interconnect to couple the memory controller to the memory modules (figure 2, and col. 3 line 55 through col. 4 line 10).

Regarding claim 12, Saulsbury discloses the arrays of tag address storage locations and the data caches organized into a plurality of ways (col. 3 lines 54-63).

Regarding claim 13, Saulsbury discloses the tag look-up operations to provide cache hit information (col. 9 line 54 through col. 10 line 21).

Regarding claim 14, Saulsbury discloses the tag look-up operations to provide cache line modified information, i.e., tag look-up operations including command to check whether the

corresponding cache line contains dirty flag, if it does, a new primary data cache line is replaced (col. 11 line 47 through col. 12 line 64).

Regarding claim 15, Saulsbury discloses the tag look-up operations to provide way information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kavipurapu (US PAT. 6,584,546) discloses highly efficient design of storage array for use in first and second cache spaces and memory subsystems (abstract).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li

September 4, 2003

MATTHEW KIM
SUPERVISORY
TECH